



**KEYSIGHT
WORLD 2020**

Data Center Technologies move toward 1\$ per Gigabit

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Agenda

- Datacom trends fueling innovation
- Optical Interconnects in 2020
- Technologies for lowering Data Center (DC) footprint
- Call to action

Datacom trends fueling innovation



Datacom trends fueling innovation

BANDWIDTH, POWER, PRICE



25%

**INTERNET TRAFFIC
CAGR**

x3 in five years (2016-2021)



50%

**WORKLOAD RUN
OUTSIDE THE
ENTERPRISE**

Computing moving in the cloud or
at the edge



99%

**99% TRAFFIC FROM
DATA CENTER**

Originated or terminated in Data
Center

Sources: Statista, Cisco Global Source Index

Hyperscale Data Center



AWS CLOUD

49 Availability Zones within 18 geographic Regions

Plans for 12 more Availability Zones and 4 more Regions

IaaS/PaaS



MICROSOFT AZURE

Available in 36 regions

Plans for 6 additional regions.

IaaS/PaaS/SaaS



IBM CLOUD

60 Data Centers in 19 countries

IaaS/PaaS



FACEBOOK

7 Mega Centers

Plans to expand 3 of the existing and add 4 new Mega Data centers

SaaS

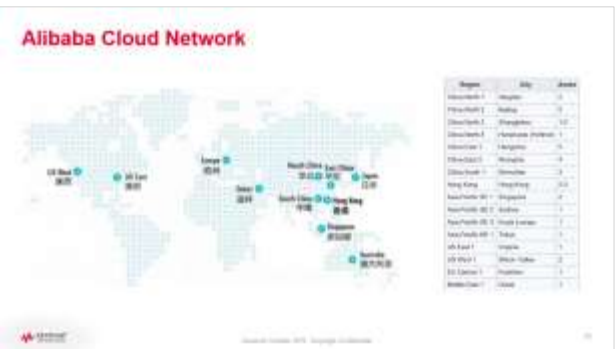


GOOGLE CLOUD

13 regions and 49 zones

Plans for 5 additional regions and 14 zones

IaaS/PaaS/SaaS



ALIBABA

7 regions and 33 zones

Plans for 4 additional regions

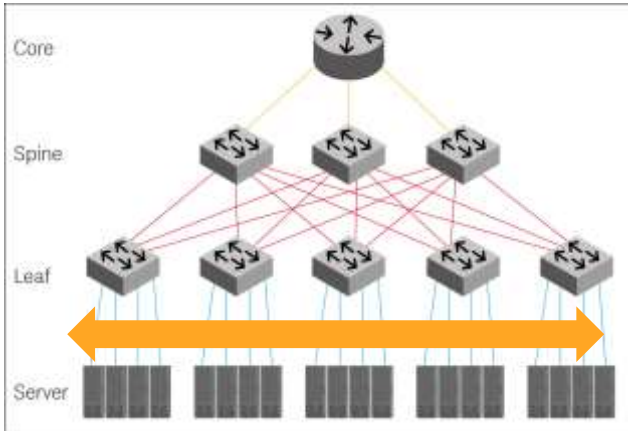
IaaS/PaaS

A look into Mega Data Centers

TRAFFIC DOMINATED BY MACHINE TO MACHINE COMMUNICATION

71%

EAST-WEST TRAFFIC



M2M in the DC

15%

NORTH-SOUTH TRAFFIC



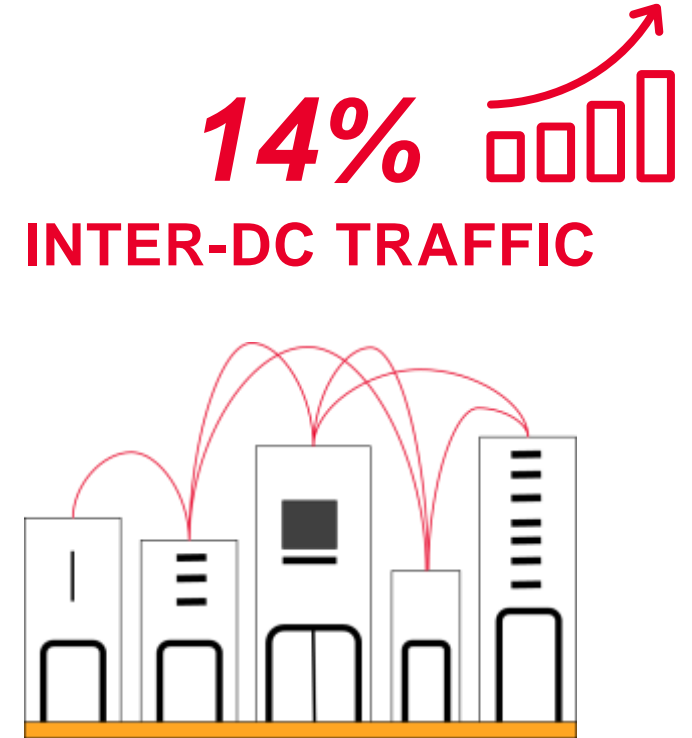
User



Cloud

14%

INTER-DC TRAFFIC



Source: Cisco Global Source Index

Data Center challenges

POWER, SPENDING, DELAY



50%

POWER CONSUMPTION FOR COOLING

>1% of WW el. Power consumption



\$152Md

DATA CENTER SPENDING ON SW & HW

Steadily increasing. Hyperscale Data Centers account for a third of the market



6%

DROP IN SALES FOR 0.1S LATENCY

Similar results from amazon & google

Source: Statista, [Northwestern University](#), Synergy research group, Yole development, [Akamai study](#)

Data Center challenges

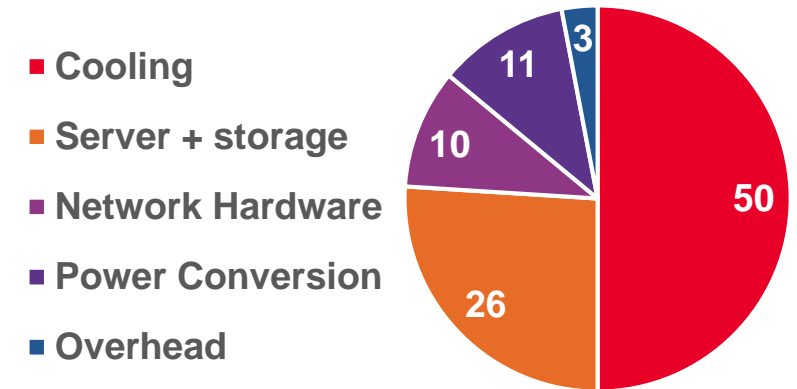
TOWARD 1PJ/BIT

- **Reduced footprint**
 - Optimized **cooling** techniques, Server **virtualization** (VMs), etc.
 - Deploying **efficient** computing & networking technologies
- **The cascade effect**
 - **1W** reduction at the component level results in **2W+** reduction at the Data Center level

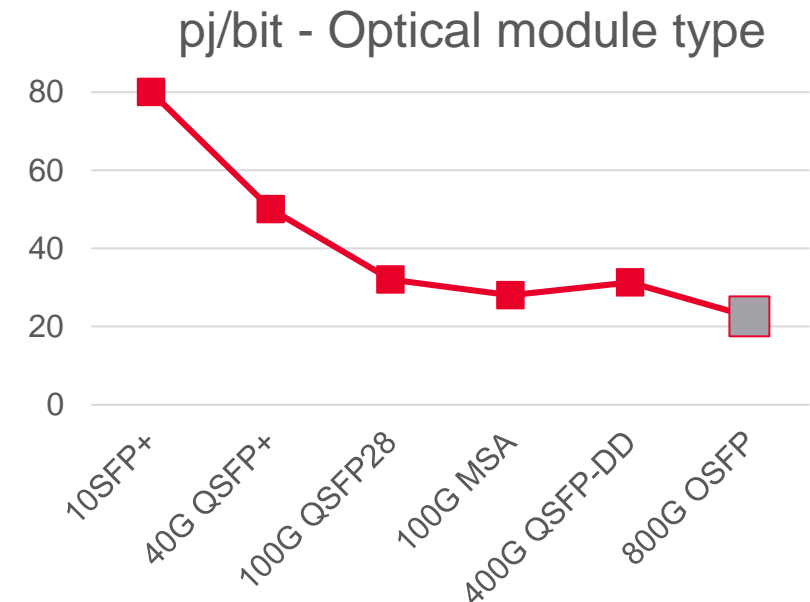
➔ 50Tb switch @ 20pj/bit = 2000Watt for populated chassis (1000Watt for optics)

NEED TO GO BELOW 5PJ/BIT

DC power consumption



Source: Yole dev



Data Center challenges

TOWARD 1\$/GB/S OPTICAL I/O

- **Reduced spending**

- Secure multi-source supply chain by
 - Enforcing **interoperability**
 - Fostering **white box** ecosystem (OCP)
- Just good-enough design with **MSAs**
- Leverage mass volume technologies
 - CMOS for consumer electronics (**Silicon Photonics**)
 - **VSCEL** for SR interconnects

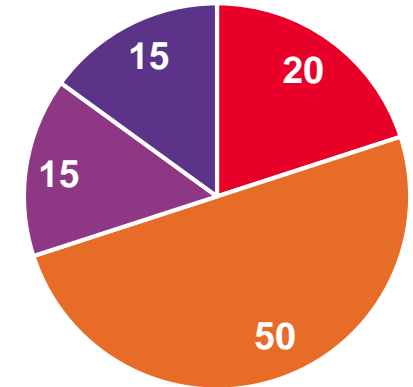


Impact of optics in networking cost is growing
(10% @10G, 30% @100G, 50% @400G)

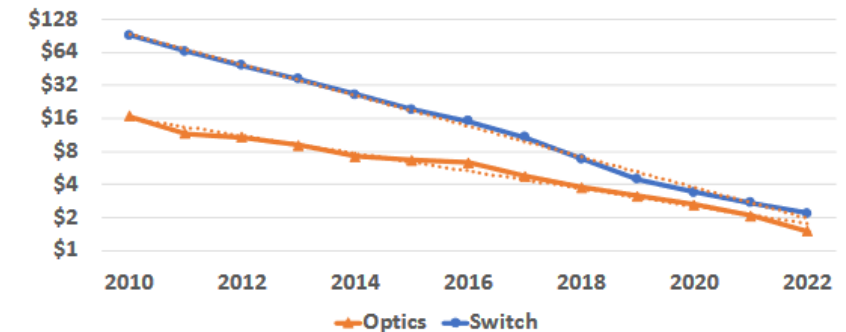
1\$/GIGABIT FOR 400G OPTICAL TRX

Estimated DC Cost

- Cooling & distr.
- Server + storage
- Networking equipment
- Power



Ethernet switch and optics cost [\$/Gbps]



Source: LightCounting, Dell'oro, Rockley Photonics

Optical Interconnects in 2020



Optical Interconnects in 2020

UNLEASHING 400G



25.6TB SWITCH

12.8Tb currently deployed at hyperscale



400G OPTICS IN THE STARTING BLOCKS

Mass deployment delayed

50% cost reduction compared to 100G

15W/module is still an issue

(100G=3W)



100G SERIAL IN THE STARTING BLOCK

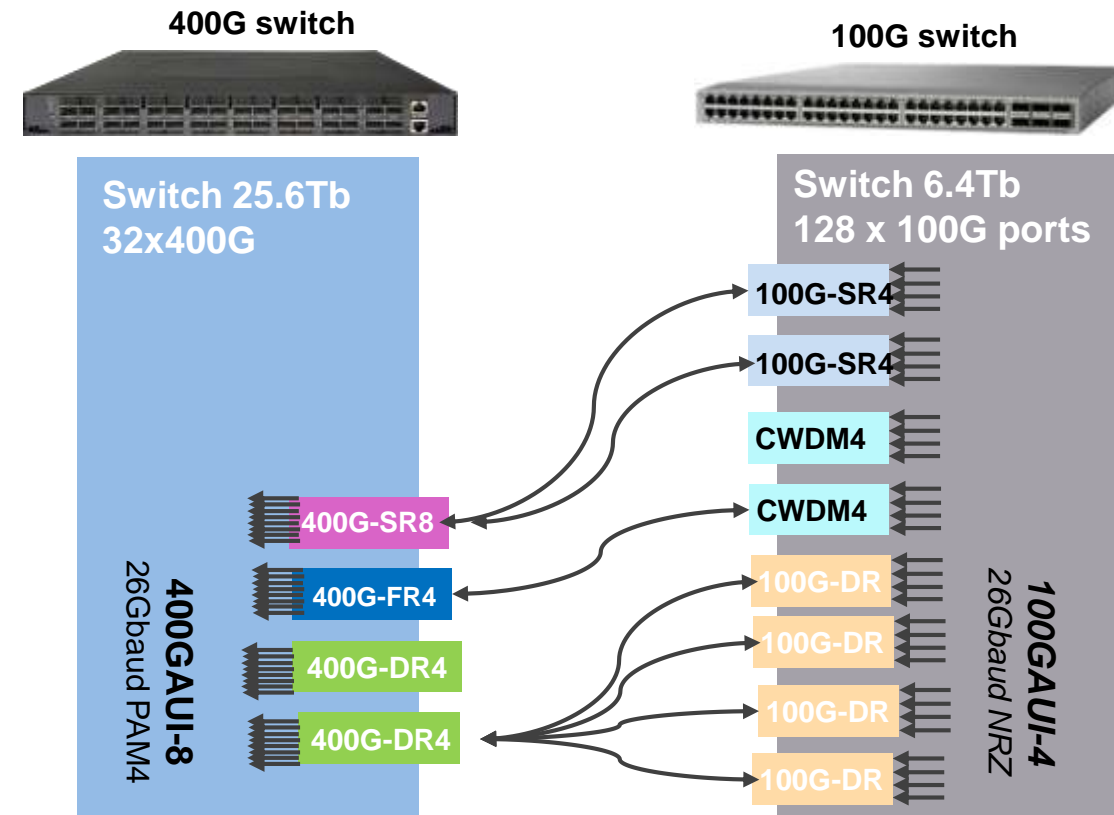
IEEE 80.23ck close to release

25.6Tb 100G SerDes-based switch ASIC by Innovium

400G deployment

400G SLOWY RAMPING

- **Status @ Hyperscale DC's** (Source LightCounting)
 - 400GbE DR4 delayed at **AWS** (chip)
 - 200GbE just started at **Facebook**
 - 2x200GbE slow start at **Google**
- **What is slowing down 400G?**
 - 100G PSM4 (<2\$/Gb) vs 400G-DR4 (~4\$/Gb)
 - <30pj/bit for CWDM4, >35pj/bit for 400G-DR4
 - Technical issues: Interoperability, margin (BER vs. FLR)

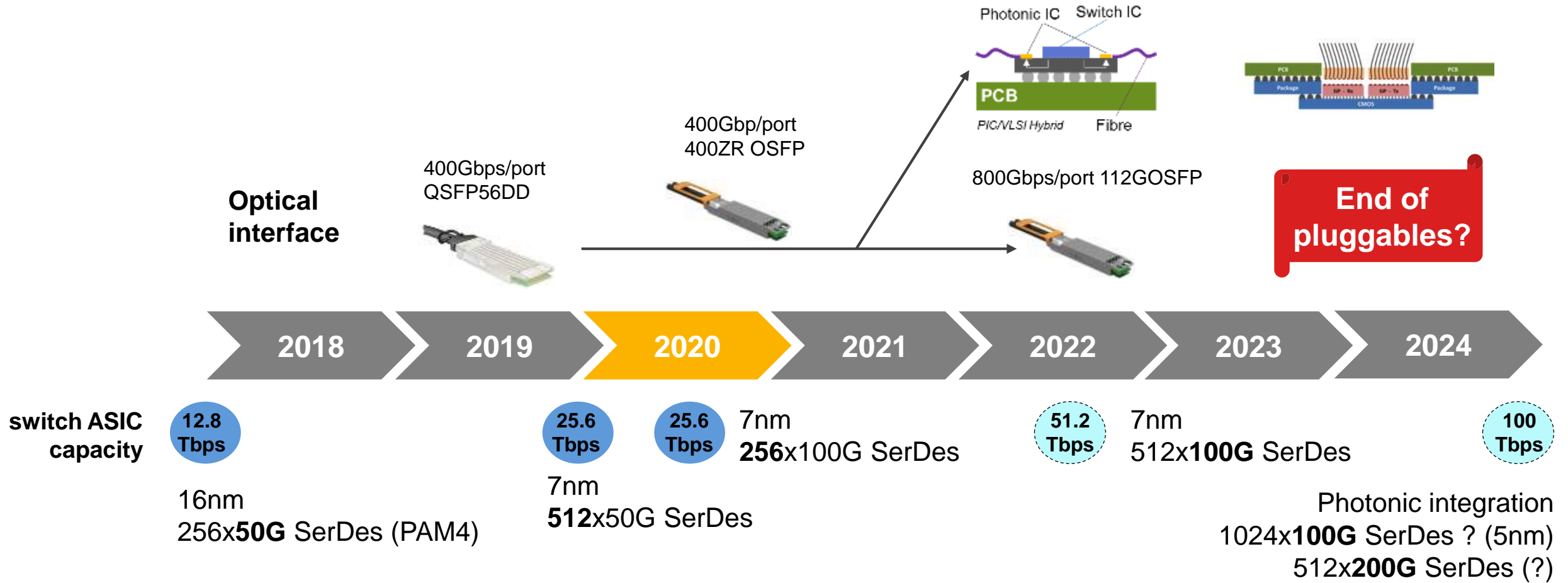


* 400G-FR4, configured 100G CWDM4 mode

* 400G-SR8, configured in 2 x 100-SR4 mode

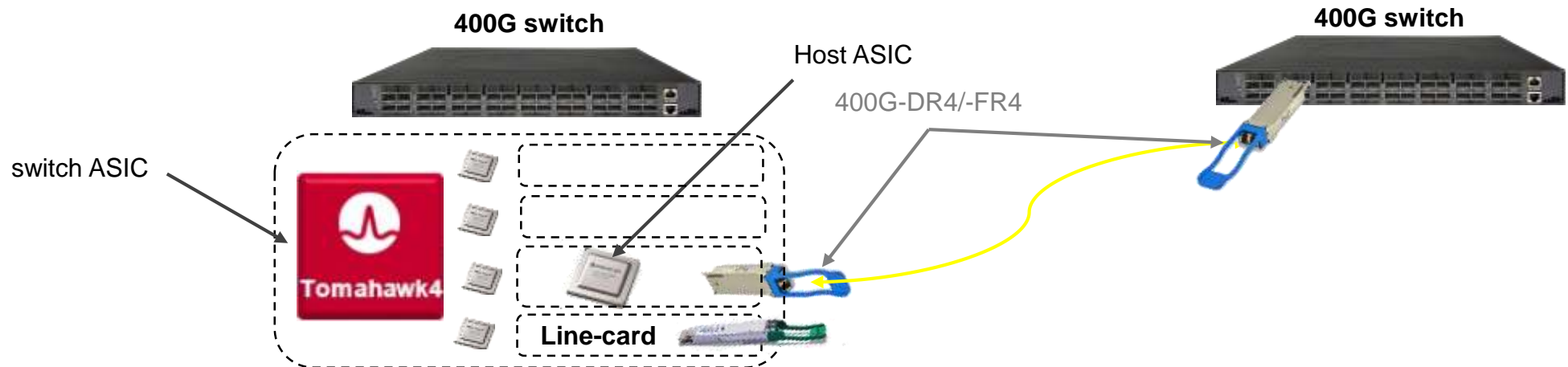
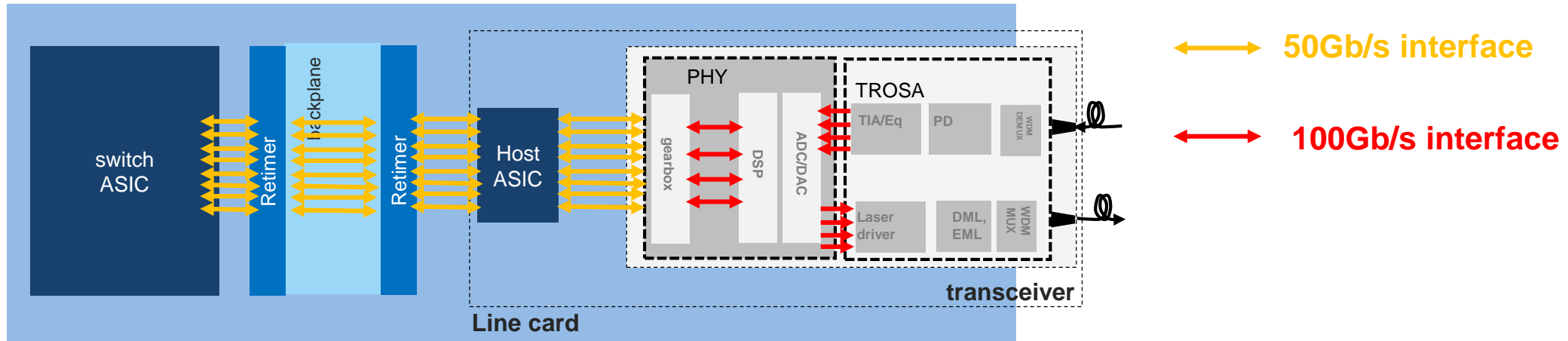
2020: Technology crossroads for R&D

SWITCH ASIC EVOLUTION



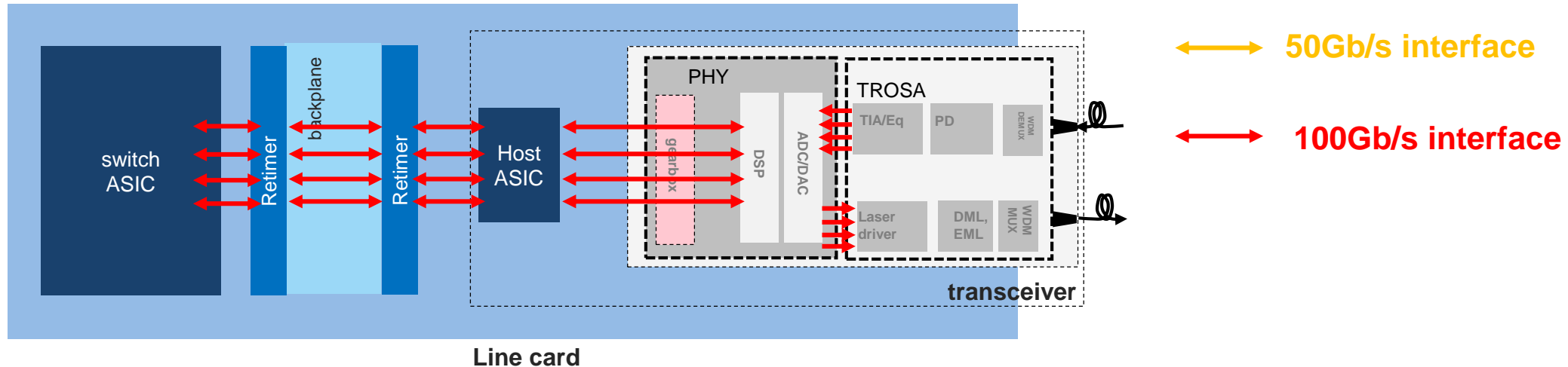
2020: Technology crossroads for R&D

100G SERIAL ELECTRICAL



2020: Technology crossroads for R&D

100G SERIAL ELECTRICAL



Standards

- IEEE 802.3ck
- OIF-CEI 5.0

Benefits

- Reduced power consumption (no gearbox)
- 800G-ready (8 lanes)

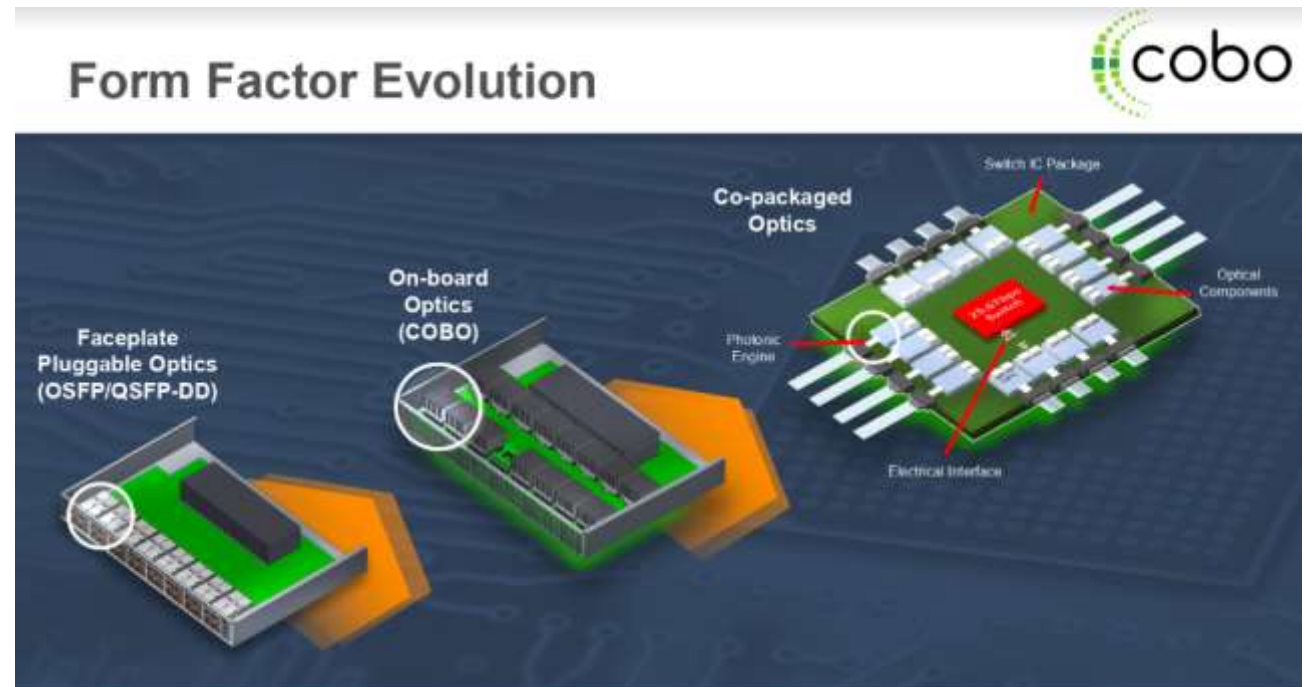
Challenges compared to 50G

- High Signal Integrity
- Higher Channel Losses & reflections
- Complex equalization (CTLE+DFE)

The rise of on-boards and co-package optics

IN A NUTSHELL

- **On-Board Optics:** Optical modules mounted on PCB
- **Co-packaged optics:** Optical engines co-packaged with switching ASIC
- **Silicon photonics:** Integration of electronics and photonic circuits in the same technology platform
- **Industry initiatives**
 - Consortium for On-Board Optics, **COBO**
 - Co-Packaged Optics Collaboration, **CPO**
 - **CWDM-MSA**
- **Some 2020 CPO announcements**
 - 12.8 Tbps switch with 1.6Tb/s optics (Intel)
 - 25.6T OptoASIC Switch system (Rockley)
 - 3.2 Tbps TOR switch (Accton, Cisco)
 - and much more ...

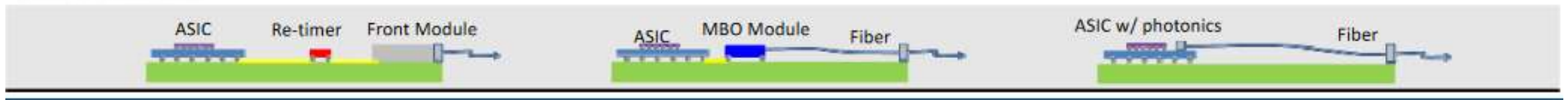


Source: COBO

Keysight World 2020 Taipei

The rise of on-boards and co-package optics

EXPECTED BENEFITS AND CHALLENGES



Source: Luxtera

- **Benefits**

- **Bring optics closer to ASICs**

- Removed or simplified re-timer, **75% power reduction** compared to classical PCB
 - Switch bandwidth **scalability**: reduced size & footprint

- **Silicon scale** (CPO only)

- Leverage well-known and rapidly scalable fabrication CMOS fab environment
 - Reduce packaging cost (80% of the total TRX cost in 2015)

- **Challenges**

- Lack of flexibility (e.g. replacing defect optical engines, fixed optical interfaces)
 - Complex thermal and mechanical design
 - Manufacturing complexity and yield (CPO only)

Technologies for lowering Data Center footprint



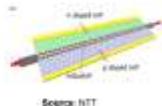
Technologies for lowering Data Center footprint

OVERVIEW

- CMOS process
- VCSEL
- Photonics structures
- Materials
- **Integrated Photonics**
 - Monolithic integration
 - Hybrid Integration

Alternative Modulator technologies

- Ring resonators
 - X10 simpler than MZM
 - X10 more efficient (0.2p vs 2pJ/bit)
- Nanophotonic
 - 2fJ/bit EO modulator
- Photonic Crystal



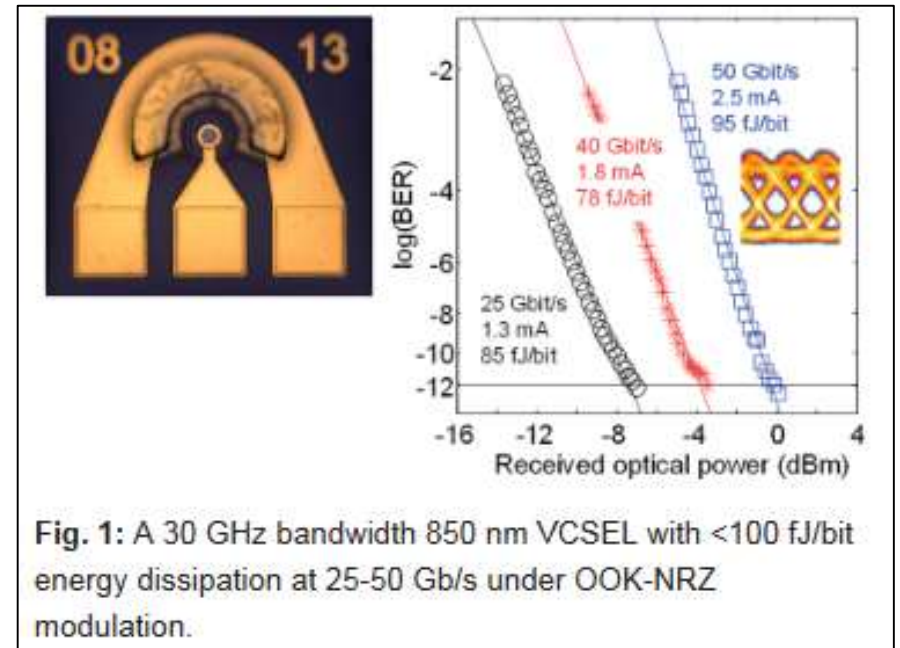
Source: NTT

Power Efficient Materials

- Phase modulators:
 - LiNbO₃: thin films bonded on silicon
 - BTO (Barium Titanate): epitaxially grown on silicon with STO buffer layer
 - PZT: sol-gel deposition on any substrate
 - EO-polymers: commercially or specially
- Amplitude modulators:
 - Graphene: layer transfer

Material	V _π (V/μm)	Insertion loss (dB/cm)	FCR _{π/2} (fJ/bit)
LiNbO ₃ (B)	30-100	10	20-40
LiNbO ₃ (P)	10	10	5-1
BariumTitanate (B)	4-10	10	5-1
Si photonic (B)	10-100	1-2	10-20
Graphene (B)	0.7-1.8	0.3-1.2	1-2

Source: M. Romagnolo et al

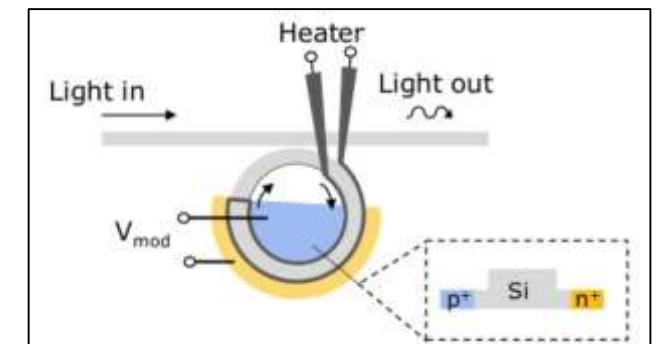
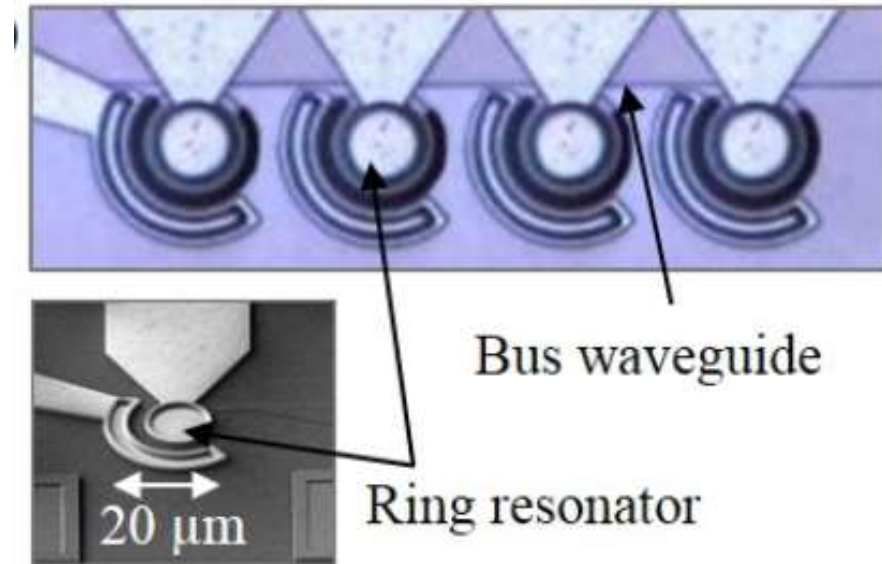


Source: A. Larsson and al.

Integrated Photonics

MONOLITIC INTEGRATION, E.G. RANOVUS

- SOI Platform
 - Heater tunes ring resonance frequency
 - QD multiwavelength laser (external)
- Benefit (quoting Ranovus)
 - 800G-3.2Tb/s per photonic engine
 - 100Gb/s (50Gbaud PAM4) modulation
 - 50% power consumption (0.2 pj/bit per ring)
 - 75% cost/Gbps reduction
 - Reduced latency

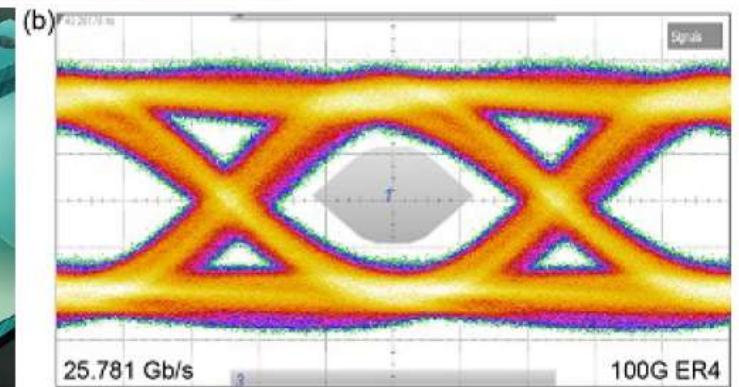
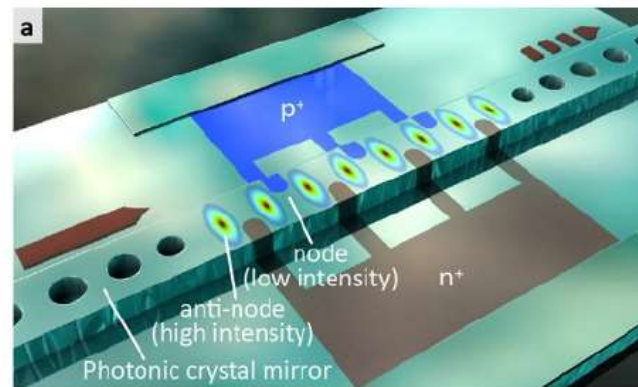
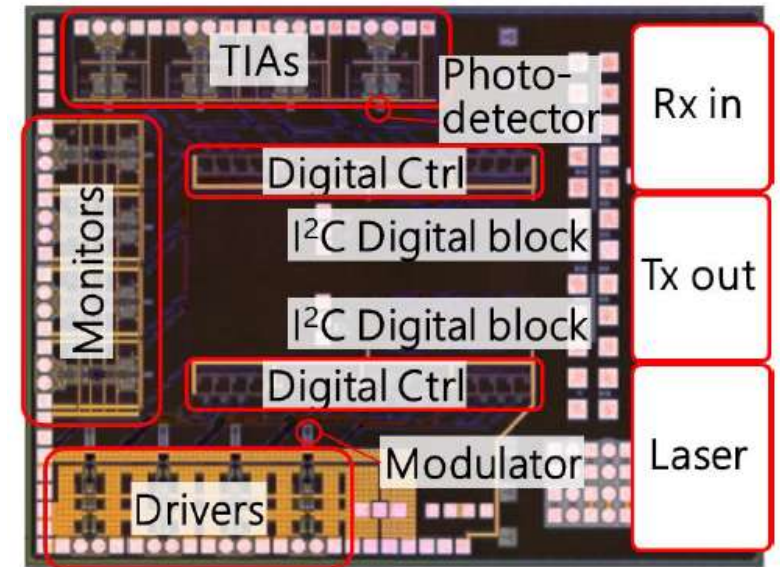


source ADVA, Ranovus

Integrated Photonics

MONOLITIC INTEGRATION, E.G. SICOYA

- SiGe-BiCMOS
 - 1D photonic crystal Fabry-perot resonator waveguide
 - Modulation achieved by carrier depletion
 - Fully integrated modulator drivers and TIAs
 - Laser coupling via gratings
- Benefit (quoting Sicoya)
 - Higher yield using mature CMOS
 - Small footprint



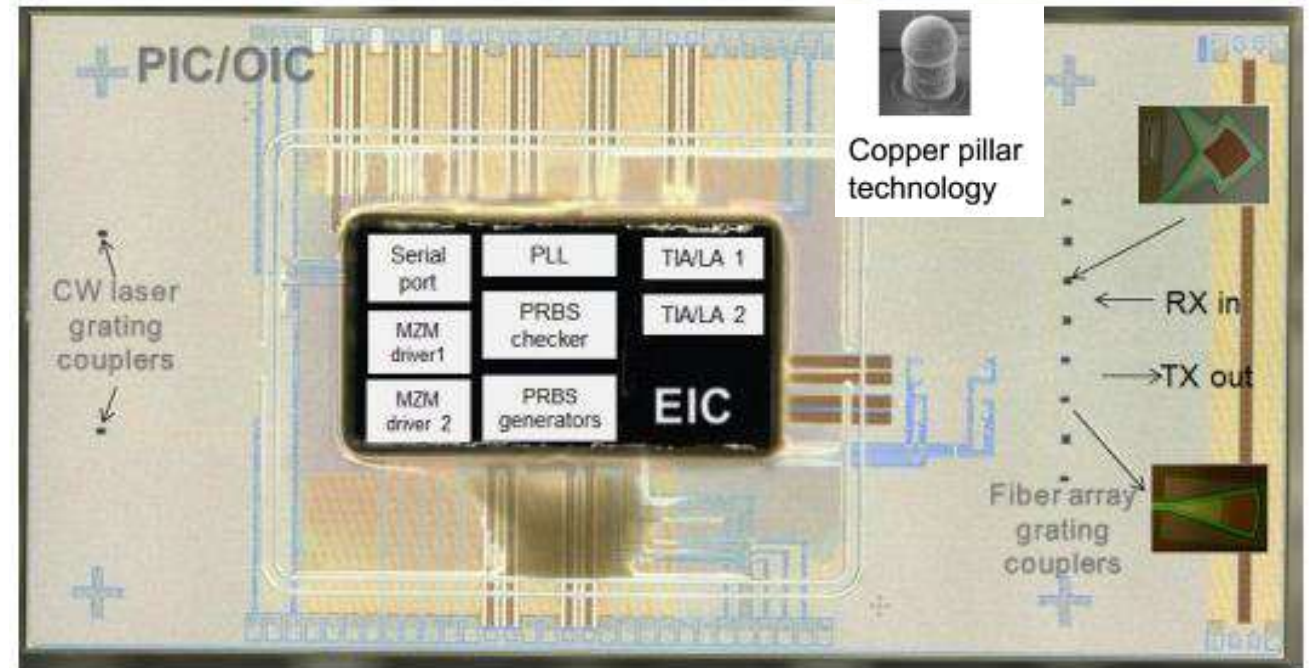
Courtesy of Abdul Rahim, ePIXfab

Integrated Photonics

HYBRID INTEGRATION, E.G. FINISAR

- Hybrid integration of electronics and photonic ICs e.g. using the copper pillar technology
- STMicroelectronics PIC25G silicon photonics technology
- Coupling from fiber and from the laser is done by using grating couplers
- Distributed loading of the transmission line electrode

O- band, 56 Gb/s @ 2Km in a CFP4 package

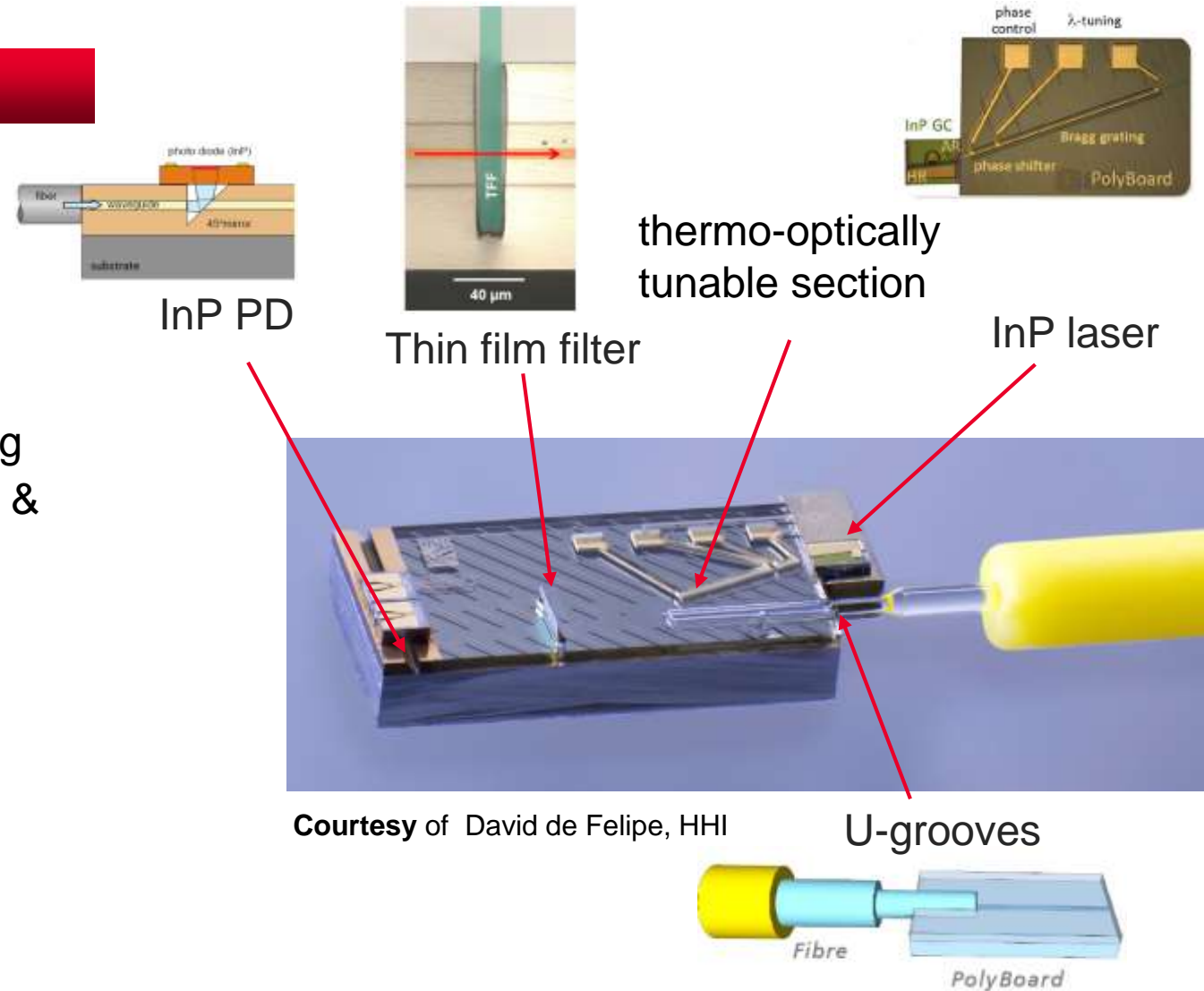


Courtesy of Abdul Rahim, ePIXfab

Integrated Photonics

HYBRID INTEGRATION, E.G. POLYMER

- Polymer for integrating technologies from different material platforms
- Key building blocks
 - Thin film element for λ and polarization filtering
 - Polymer thermo-optically tunable bragg grating & phase shifter
 - PD, laser (Inp; GaAs)
 - Modulator (SiNx, LiNbO3)
- TERIPHIC – EU funded project
 - 800G transceivers
 - power consumption reduced by 50%
 - 0.3 €/Gb/s.



Summary & Resources

- Insatiable demand for capacity and switching bandwidth in the Data Center will continue to fuel innovation - 100Tb switch in 2025!
- Scaling current paradigm to 50Tb switch seems very challenging - Sub\$/bit and 5pj/bit achievable with pluggable?
- Resources and [related Keysight solutions](#)
 - **Unlocking 400G by**
 - Increasing manufacturing throughput with fast and reliable T&M solution - [KS8108A](#)
 - Ensuring interoperability by FEC-aware compliance testing - [N4891A](#)
 - Reducing impact of yield with early functional on-wafer test - [N7700210C](#)
 - **Paving the way for 1.6TbE by**
 - Investigating 200G/lane implementation – [M8194A](#)
 - Measuring channel beyond 60GHz – [N1930B](#)
 - Characterizing optical components up to 110GHZ - [N4372E](#)



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